WHAT IS CLAIMED IS:

- 1 1. A method of forming a gate electrode of a multiple-gate transistor comprising:
- 2 providing a semiconductor structure including a semiconductor fin overlying an insulator
- 3 layer, and a gate dielectric overlying at least a portion of the semiconductor fin;
- forming a first gate electrode material overlying the gate dielectric;
- forming a second gate electrode material overlying the first gate electrode material;
- forming a patterned mask over the second gate electrode material;
- 7 etching the second gate electrode material; and
- 8 etching the first gate electrode material.
- 1 2. The method of claim 1 further comprising planarizing a non-planar top surface of the
- 2 second gate electrode material to form a planarized top surface.
- 1 3. The method of claim 2 wherein the non-planar top surface is substantially conformal with
- 2 respect to the semiconductor structure.
- 1 4. The method of claim 2 wherein planarizing a non-planar top surface comprises
- 2 performing a chemical mechanical polishing process.
- 1 5. The method of claim 2 wherein the planarizing step exposes the first gate electrode
- 2 material.
- 1 6. The method of claim 1 further comprising forming source and drain regions in the
- 2 semiconductor fin.

- 1 7. The method of claim 1 further comprising:
- 2 forming spacers on the sides of the gate electrode;
- 3 performing selective epitaxy on the portions of the semiconductor fin not covered by the
- 4 gate electrode; and
- 5 forming source and drain regions.
- 1 8. The method of claim 1 wherein the semiconductor fin comprises a silicon fin.
- 1 9. The method of claim 1 wherein the semiconductor fin comprises a silicon and germanium
- 2 fin.
- 1 10. The method of claim 1 wherein the patterned mask comprises a mask material selected
- 2 from a group comprising of silicon nitride, silicon oxynitride, silicon oxide, and photoresist, and
- 3 combinations thereof.
- 1 11. The method of claim 1 wherein etching the second gate electrode material comprises
- 2 performing a plasma etching process.
- 1 12. The method of claim 11 wherein the plasma etching process etches the second gate
- 2 electrode material at a faster etch rate than it etches the first gate electrode material.
- 1 13. The method of claim 1 wherein the etching of the second gate electrode material stops on
- 2 the first gate electrode material.
- 1 14. The method of claim 1 wherein etching the first gate electrode material comprises
- 2 performing a plasma etching process or a wet etching process.

- 1 15. The method of claim 1 wherein the gate dielectric comprises silicon oxide.
- 1 16. The method of claim 1 wherein the gate dielectric comprises silicon oxynitride.
- 1 17. The method of claim 1 wherein the gate dielectric comprises a high permittivity material.
- 1 18. The method of claim 17 where the gate dielectric comprises a material selected from the
- 2 group consisting of lanthanum oxide, aluminum oxide, hafnium oxide, hafnium oxynitride, and
- 3 zirconium oxide, and combinations thereof.
- 1 19. The method of claim 17 wherein the gate dielectric comprises of high permittivity
- 2 materials with relative permittivity greater than about 5.
- 1 20. The method of claim 1 wherein the gate dielectric has a thickness less than about 10
- 2 angstroms.
- 1 21. The method of claim 1 wherein the first gate electrode material is selected from a group
- 2 comprising of poly-Si, poly-SiGe, a metallic nitride, a metallic silicide, or a metal, or
- 3 combinations thereof.
- 1 22. The method of claim 1 wherein the second gate electrode material is selected from a
- 2 group comprising of poly-Si, poly-SiGe, a metallic nitride, a metallic silicide, or a metal, or
- 3 combinations thereof.

- 1 23. The method of claim 1 wherein the first gate electrode material comprises a metallic
- 2 nitride, and the second gate electrode material is selected from the group comprising of poly-Si,
- 3 poly-SiGe, a metallic nitride, a metallic silicide, and a metal.
- 1 24. The method of claim 1 wherein the first gate electrode material comprises a metal, and
- 2 the second gate electrode material is selected from a group comprising of poly-Si, poly-SiGe, a
- 3 metallic nitride, a metallic silicide, or a metal, or combinations thereof.
- 1 25. The method of claim 1 wherein the multiple-gate transistor is a triple-gate transistor.
- 1 26. The method of claim 1 wherein the multiple-gate transistor is a double-gate transistor.

- 1 27. A multiple-gate transistor structure comprising:
- 2 a semiconductor fin overlying an insulator layer;
- a gate dielectric overlying at least a portion of the semiconductor fin;
- a gate electrode overlying the gate dielectric, the gate electrode comprising a first gate
- 5 electrode material underlying a second gate electrode material, wherein the first gate electrode
- 6 material has a thickness of less than about 500 angstroms; and
- 7 source and drain regions in portions of the semiconductor fin oppositely adjacent to said
- 8 gate electrode.
- 1 28. The structure of claim 27 wherein the first gate electrode material and the second gate
- 2 electrode material are selected from a group consisting of poly-Si, poly-SiGe, a metallic nitride,
- a metallic silicide, and a metal, and combinations thereof.
- 1 29. The structure of claim 27 wherein the first gate electrode material comprises a metallic
- 2 nitride, and the second gate electrode material is selected from a group consisting of poly-Si,
- 3 poly-SiGe, a metallic nitride, a metallic silicide, and a metal, and combinations thereof.
- 1 30. The structure of claim 27 wherein the first gate electrode material comprises a metal, and
- 2 the second gate electrode material is selected from a group consisting of poly-Si, poly-SiGe, a
- 3 metallic nitride, a metallic silicide, and a metal, and combinations thereof.
- 1 31. The structure of claim 27 wherein the second gate electrode material has a substantially
- 2 planar top surface.

- 1 32. The structure of claim 27 and further comprising spacers disposed on the sides of the gate
- 2 electrode.
- 1 33. The structure of claim 27 wherein the semiconductor fin comprises silicon.
- 1 34. The structure of claim 27 wherein the semiconductor fin comprises silicon and
- 2 germanium.
- 1 35. The structure of claim 27 wherein the semiconductor structure further comprises an
- 2 etchant mask overlying the semiconductor fin.
- 1 36. The structure of claim 27 wherein the insulator layer is recessed, resulting in a notch at
- 2 the base of the semiconductor fin.
- 1 37. The structure of claim 27 wherein the gate dielectric comprises silicon oxide.
- 1 38. The structure of claim 27 wherein the gate dielectric comprises silicon oxynitride.
- 1 39. The structure of claim 27 wherein the gate dielectric comprises a high permittivity
- 2 material with relative permittivity greater than 5.
- 1 40. The structure of claim 39 wherein the gate dielectric comprises a material selected from
- the group consisting of lanthanum oxide, aluminum oxide, hafnium oxide, hafnium oxynitride,
- and zirconium oxide, and combinations thereof.
- 1 41. The structure of claim 27 wherein the gate dielectric has a thickness of less than about 10
- 2 angstroms.

- 1 42. The structure of claim 27 wherein the multiple-gate transistor is a triple-gate transistor.
- 1 43. The structure of claim 27 wherein the multiple-gate transistor is a double-gate transistor.

- 1 44. A method of forming semiconductor device, the method comprising:
- 2 providing a semiconductor-on-insulator substrate;
- forming a semiconductor fin on the semiconductor-on-insulator substrate;
- forming a gate dielectric over at least a portion of the semiconductor fin;
- forming a first gate electrode material overlying the gate dielectric;
- forming a second gate electrode material overlying the first gate electrode material;
- 7 planarizing the second gate electrode material;
- 8 etching the second gate electrode material selectively with respect to first gate electrode
- 9 material; and
- 10 etching the first gate electrode material.
- 1 45. The method of claim 44 and further comprising forming source and drain regions in the
- 2 semiconductor fin after etching the first gate electrode material.
- 1 46. The method of claim 45 and further comprising forming sidewall spacers along sidewalls
- 2 of the semiconductor fin prior to forming source and drain regions.
- 1 47. The method of claim 44 wherein planarizing the second gate electrode material comprises
- 2 performing a chemical mechanical polishing process.
- 1 48. The method of claim 47 wherein the planarizing step exposes the first gate electrode
- 2 material.
- 1 49. The method of claim 44 wherein the gate dielectric comprises a high permittivity material
- 2 with a relative permittivity greater than about 5.

- 1 50. The method of claim 44 wherein the first gate electrode material is selected from a group
- 2 comprising of poly-Si, poly-SiGe, a metallic nitride, a metallic silicide, or a metal, or
- 3 combinations thereof.
- 1 51. The method of claim 44 wherein the second gate electrode material is selected from a
- 2 group comprising of poly-Si, poly-SiGe, a metallic nitride, a metallic silicide, or a metal, or
- 3 combinations thereof.
- 1 52. The method of claim 51 wherein the first gate electrode material comprises a metallic
- 2 nitride, and the second gate electrode material is selected from the group comprising of poly-Si,
- 3 poly-SiGe, a metallic nitride, a metallic silicide, and a metal.

- 1 53. A method of forming a multiple gate transistor device, the method comprising:
- 2 providing a semiconductor structure including a semiconductor fin overlying an insulator
- 3 layer, and a gate dielectric overlying at least a portion of the semiconductor fin;
- 4 forming a gate electrode material over the gate dielectric;
- 5 forming a planarizing layer over the gate electrode material;
- etching the planarizing layer and the gate electrode material to form a gate electrode layer
- 7 with a substantially planar upper surface; and
- 8 patterning and etching the gate electrode material to form a gate electrode.
- 1 54. The method of claim 53 wherein etching the planarizing layer and the gate electrode
- 2 material comprises performing an etch back process.
- 1 55. The method of claim 53 wherein etching the planarizing layer and the gate electrode
- 2 material comprises performing a chemical-mechanical polish process.
- 1 56. The method of claim 53 wherein the planarizing layer comprises a dielectric layer.
- 1 57. The method of claim 53 and further comprising forming a second gate electrode layer
- 2 over the gate dielectric before forming the gate electrode material.
- 1 58. The method of claim 53 further comprising forming source and drain regions in the
- 2 semiconductor fin.
- 1 59. The method of claim 53 further comprising:
- 2 forming spacers on the sides of the gate electrode;
- performing selective epitaxy on the portions of the semiconductor fin not covered by the

- 4 gate electrode; and
- 5 forming source and drain regions.
- 1 60. The method of claim 53 wherein the semiconductor fin comprises a silicon fin.
- 1 61. The method of claim 53 wherein the semiconductor fin comprises a silicon and
- 2 germanium fin.
- 1 62. The method of claim 53 wherein the gate dielectric comprises silicon oxide.
- 1 63. The method of claim 53 wherein the gate dielectric comprises silicon oxynitride.
- 1 64. The method of claim 53 wherein the gate dielectric comprises of high permittivity
- 2 materials with relative permittivity greater than about 5.
- 1 65. The method of claim 64 where the gate dielectric comprises a material selected from the
- 2 group consisting of lanthanum oxide, aluminum oxide, hafnium oxide, hafnium oxynitride, and
- 3 zirconium oxide, and combinations thereof.

- 1 66. The method of claim 53 wherein the gate dielectric has a thickness less than about 10
- 2 angstroms.
- 1 67. The method of claim 53 wherein the first gate electrode material is selected from a group
- 2 comprising of poly-Si, poly-SiGe, a metallic nitride, a metallic silicide, or a metal, or
- 3 combinations thereof.
- 1 68. The method of claim 53 wherein the planarizing layer is formed from a material selected
- 2 from the group consisting of silicon rich oxide, spin-on glass, silicon oxide, and doped glass.
- 1 69. The method of claim 53 wherein the planarizing layer comprises silicon rich oxide and
- 2 the gate electrode material comprises polysilicon.